THAT WHICH IS CLAIMED IS:

1. A content addressable memory (CAM) device, comprising:

a CAM array block having a first row of CAM cells therein that comprises:

a first match line segment that is electrically coupled to a first segment of CAM cells in the first row;

a second match line segment that is electrically coupled to a second segment of CAM cells in the first row;

a pseudo-ground line segment that is electrically connected to the first and second segment of CAM cells; and

a speed adjustable match line signal repeater that is configured to detect and propagate a miss signal transition from the first match line segment to the second match line segment during a search operation.

2. The CAM device of Claim 1, wherein said match line signal repeater is configured to propagate the miss signal transition in-sync with a high-to-low transition of the pseudo-ground line segment.

3. The CAM device of Claim 2, wherein said match line signal repeater is configured to propagate the miss signal transition in-sync with a high-to-low transition of the pseudo-ground line segment from a maximum high voltage of (Vdd-Vth) to a low voltage of Vss, where Vdd is a power supply voltage, Vth is a threshold voltage of an NMOS transistor and Vss is a reference supply voltage.

4. The CAM device of Claim 1, wherein said match line signal repeater comprises an inverter having an input that is electrically coupled to the first match line segment, an output and a sensitivity control terminal.

5. The CAM device of Claim 4, wherein said match line signal repeater comprises a voltage-controlled impedance element that is electrically coupled in series between the sensitivity control terminal of the inverter and a reference supply line.

6. The CAM device of Claim 5, wherein the voltage-controlled impedance element comprises an NMOS bias transistor having a gate electrode that receives an adjustable N-bias voltage; and wherein the N-bias voltage has a magnitude that disposes the NMOS bias transistor in its linear region of operation.

7. The CAM device of Claim 6, wherein said match line signal repeater further comprises an NMOS pull-down transistor having a first current carrying terminal that is electrically connected to the sensitivity control terminal, a second current carrying terminal that is electrically connected to the reference supply line and a gate terminal that is responsive to an evaluation control signal.

8. The CAM device of Claim 4, further comprising a precharge support circuit that is electrically coupled between the first match line segment and a power supply line, said precharge support circuit having a first control input that is electrically coupled to the output of the inverter.

9. The CAM device of Claim 8, wherein the precharge support circuit comprises first and second PMOS pull-up transistors that are electrically connected in series between the first match line segment and the power supply line.

10. The CAM device of Claim 9, wherein a gate electrode of the first PMOS pull-up transistor is electrically coupled to the first control input of the precharge support circuit.

11. The CAM device of Claim 10, wherein a gate electrode of the second PMOS pull-up transistor is responsive to a P-bias voltage having a magnitude that disposes the second PMOS bias transistor in its linear region of operation.

12. The CAM device of Claim 4, wherein said match line signal repeater comprises:

an NMOS pull-down transistor having a gate that is electrically coupled to the output of the inverter, a first current carrying terminal that is electrically connected to the second match line segment and second current carrying terminal that is electrically connected to the pseudo-ground line segment; and

a PMOS pull-up transistor having a gate that is responsive to a control signal, a first current carrying terminal that is electrically connected to the second match line segment and a second current carrying terminal that is electrically connected to a power supply line.

13. The CAM device of Claim 5, wherein said match line signal repeater comprises an NMOS pull-down transistor having a gate that is electrically coupled to the output of the inverter and a first current carrying terminal that is electrically connected to the second match line segment.

14. The CAM device of Claim 3, wherein said match line signal repeater comprises an inverter having an input that is electrically coupled to the first match line segment, an output and a sensitivity control terminal.

15. The CAM device of Claim 5, wherein said match line signal repeater further comprises an NMOS pull-down transistor having a first current carrying terminal electrically connected to the sensitivity control terminal, a second current carrying terminal electrically connected to the reference supply line and a gate terminal that is responsive to an evaluation control signal.

16. A content addressable memory (CAM) device, comprising:

a CAM array block having a first row of CAM cells therein that comprises:

a first match line segment that is electrically coupled to a first segment of CAM cells in the first row;

a second match line segment that is electrically coupled to a second segment of CAM cells in the first row; and

a speed adjustable match line signal repeater that is configured to detect and propagate a miss signal transition from the first match line segment to the second match line segment during a search operation.

17. A content addressable memory (CAM) device, comprising:

a CAM array block having a pair of rows of CAM cells therein that comprise:

first and second match line segments associated with a first row of CAM cells;

third and fourth match line segments associated with a second row of CAM cells;

a pseudo-ground line segment that is electrically coupled to the first and second rows of CAM cells;

a first match line signal repeater that is electrically coupled to the first and second match line segments and the pseudo-ground line segment, said first match line signal repeater configured to detect and propagate a first miss signal transition from the first match line segment to the second match line segment during a search operation; and

a second match line signal repeater that is electrically coupled to the third and fourth match line segments and the pseudo-ground line segment, said second match line signal repeater configured to detect and propagate a second miss signal transition from the third match line segment to the fourth match line segment during the search operation.

18. The CAM device of Claim 17, wherein the first match line signal repeater comprises:

an NMOS pull-down transistor having a first current carrying terminal electrically connected to the second match line segment and a second current carrying terminal electrically connected to the pseudo-ground line segment; and

an inverter having an input that is electrically coupled to the first match line segment and an output that is electrically connected to a gate terminal of the NMOS pull-down transistor.

19. The CAM device of Claim 18, further comprising a precharge support circuit that is electrically coupled between the first match line segment and a power supply line, said precharge support circuit comprising a first PMOS pull-up transistor having a first current carrying terminal electrically connected to the first match line segment and a gate terminal electrically coupled an output of said inverter.

20. The CAM device of Claim 19, wherein the precharge support circuit further comprises a second PMOS pull-up transistor having a first current carrying terminal electrically connected to a second current carrying terminal of the first PMOS pull-up transistor, a second current carrying terminal electrically connected to the power supply line and a gate terminal that is responsive to a P-bias voltage having a magnitude that disposes the second PMOS pull-up transistor in a linear mode of operation.

21. A content addressable memory (CAM) device, comprising:

a CAM array having a first row of CAM cells therein that comprises:

a first match line segment that is electrically coupled to a first segment of CAM cells in the first row;

a second match line segment that is electrically coupled to a second segment of CAM cells in the first row;

a pseudo-ground line segment that is electrically connected to the first and second segments of CAM cells; and

a speed adjustable match line signal repeater that is configured to detect and propagate a miss signal transition from the first match line segment to the second match line segment in-sync with a high-to-low transition of said pseudo-ground line segment during a search operation.

22. A method of operating a content addressable memory (CAM) array, comprising the step of:

writing a xR segment of a first row in the CAM array with a xR segment of a first write word while concurrently searching a xS segment of the same CAM array with a xS segment of a first search word.

23. The method of Claim 22, wherein said step of writing a xR segment of a first row in the CAM array is preceded by the step of searching a xR segment of the CAM array with a xR segment of the first search word.

24. The method of Claim 23, wherein said step of writing a xR segment of a first row in the CAM array is followed by the step of searching the xR segment of the CAM array with a xR segment of a second search word while concurrently writing a xS segment of the first row with a xS segment of the first write word.

25. A method of operating a content addressable memory (CAM) array, comprising the step of:

reading a xR segment of a first row in the CAM array while concurrently searching a xS segment of the same CAM array with a xS segment of a first search word.

26. The method of Claim 25, wherein said step of reading a xR segment of a first row in the CAM array is preceded by the step of searching a xR segment of the CAM array with a xR segment of the first search word.

27. The method of Claim 26, wherein said step of reading a xR segment of a first row in the CAM array is followed by the step of searching the xR segment of the CAM array with a xR segment of a second search word while concurrently reading a xS segment of the first row.

28. A method of operating a content addressable memory (CAM) array, comprising the step of:

writing a xR segment of a first row in the CAM array with a xR segment of a first write word while concurrently searching a xS segment of the CAM array with a xS segment of a first search word and reading a xT segment of a second row in the CAM array.

29. A method of operating a content addressable memory (CAM) array, comprising the step of:

writing a xR segment of a first row in the CAM array with a xR segment of a first write word while concurrently writing a xS segment of a second row in the same CAM array.

30. A content addressable memory (CAM) array, comprising:

a first match line segment associated with a first row of CAM cells in the CAM array;

an inverter having an input electrically coupled to said first match line segment; and

a match line precharge support circuit comprising a first PMOS transistor having a gate terminal electrically coupled to an output of said inverter, a first current carrying terminal that is electrically coupled to said first match line segment and a second current carrying terminal that is electrically coupled to a power supply line.

31. The CAM array of Claim 30, wherein said match line precharge support circuit further comprises:

a second normally-on PMOS transistor having a first current carrying terminal that is electrically connected to the second current carrying terminal of the first PMOS transistor and a second current carrying terminal that is electrically connected to the power supply line.

32. The CAM array of Claim 30, wherein said match line precharge support circuit further comprises:

a second normally-on PMOS transistor having a first current carrying terminal that is electrically connected to the first match line segment and a second current carrying terminal that is electrically connected to the first current carrying terminal of said first PMOS transistor.

33. The CAM array of Claim 31, wherein said second normally-on PMOS transistor has a gate terminal that is responsive to a P-bias voltage having a magnitude sufficient to maintain said second normally-on PMOS transistor in a linear mode of operation.

34. The CAM array of Claim 30, wherein a pull-down path of said inverter comprises:

a first NMOS pull-down transistor having a gate terminal that is electrically connected to the input of said inverter and a drain that is electrically connected to the output of said inverter; and

a second NMOS pull-down transistor having a gate terminal that is responsive to an N-bias voltage having a magnitude sufficient to maintain said second NMOS pull-down transistor in a linear mode of operation, a drain that is electrically connected to a source of said first NMOS pull-down transistor and a source that is electrically connected to a reference supply line.

35. A method of operating a content addressable memory (CAM) array, comprising the steps of:

precharging a first match line segment and a first pseudo-ground line segment associated with a row of CAM cells in the CAM array to maximum voltages of V_{ml} and (V_{ml}-α), respectively, during a precharge operation, where $0.1(V_{ml}) < \alpha < \frac{1}{2}V_{ml}$; and

searching the row of CAM cells by switching the precharged first pseudo-ground line segment high-to-low and evaluating the first match line segment to determine whether a matching entry is present in the row of CAM cells.

36. The method of Claim 35, wherein said precharging step comprises precharging the first pseudo-ground line segment through an NMOS pull-up transistor having a threshold voltage equal to Vth, where Vth equals α.

37. The method of Claim 36, wherein the voltage V_{ml} equals a power supply voltage (Vdd).

38. The method of Claim 37, wherein said precharging step further comprises concurrently precharging a second pseudo-ground line segment associated with the row of CAM cells to a maximum voltage of V_{ml}.

39. The method of Claim 38, wherein evaluating the first match line segment to determine whether a matching entry is present in the row of CAM cells comprises performing a boolean NOR operation on a signal derived from the first match line segment and a signal derived from the second pseudo-ground line segment.

40. The method of Claim 39, wherein the signal derived from the first match line segment equals /ML, where "/" represents an inversion operation.

41. A content addressable memory (CAM) array, comprising:

a match line segment ML associated with a first row of CAM cells in the CAM array;

a pseudo-ground line segment PGND associated with the first row of CAM cells; and

a match line signal detector that is electrically coupled to said match line segment ML and said pseudo-ground line segment PGND, said match line signal detector having a NOR gate therein that is configured to identify a matching entry in the first row only when /PGND×ML=1 during a search operation.

42. The CAM array of Claim 41, wherein said match line signal detector comprises a latch that is responsive to a capture control signal.

43. The CAM array of Claim 42, wherein an output of the NOR gate is electrically coupled to a data input of the latch.

44. The CAM array of Claim 43, wherein the NOR gate has a first input electrically coupled to the pseudo-ground line segment PGND.

45. The CAM array of Claim 44, further comprising an inverter having an input electrically coupled to the match line segment and an output electrically connected to a second input of the NOR gate.

46. The CAM array of Claim 42, wherein the NOR gate is responsive to the capture control signal.

47. The CAM array of Claim 46, wherein the NOR gate comprises an NMOS control transistor and a PMOS control transistor having respective gate terminals that are responsive to opposite versions of the capture control signal.

48. A method of operating a content addressable memory (CAM) array, comprising the step of:

precharging match and pseudo-ground line segments in a xR segment of the CAM array while concurrently evaluating match conditions in a xS segment of the same CAM array during a first search operation.

49. The method of Claim 48, wherein said precharging step is followed by the step of:

precharging match and pseudo-ground line segments in the xS segment of the CAM array while concurrently evaluating match conditions in the xR segment of the CAM array during a second search operation.

50. The method of Claim 49, wherein S is about three times greater than R.

51. A method of operating a content addressable memory (CAM) array, comprising the step of:

precharging match and pseudo-ground line segments in a xR segment of the CAM array;

evaluating partial match conditions between a xR portion of a first search word and partial entries in the xR segment of the CAM array, in-sync with pulling the precharged pseudo-ground line segments in the xR segment high-to-low;

precharging match and pseudo-ground line segments in a xS segment of the CAM array; and

evaluating final match conditions between a xS portion of the first search word and partial entries in the xS segment of the CAM array, in-sync with pulling high-to-low only those pseudo-ground line segments in the xS segment that are associated with a row having a partial match in the xR segment during said step of evaluating partial match conditions.

52. The method of Claim 51, wherein each of the pseudo-ground line segments in the xS segment of the CAM array is shared by CAM cells in at least two rows of the CAM array.

53. A content addressable memory (CAM) array, comprising:

a row of CAM cells having a plurality of match line segments and a plurality of pseudo-ground line segments therein that are configured to swing rail-to-rail (Vss-to-Vdd) and rail-to-subrail (Vss-to-(Vdd-α)), respectively, during search operations, where $0.1(Vdd) < \alpha < 0.5(Vdd)$.

54. The CAM array of Claim 53, wherein said row further comprises a final pseudo-ground line segment that is configured to swing rail-to-rail during search operations.

55. A content addressable memory (CAM) array, comprising:

a row of CAM cells having a first word line segment and a first match line segment therein that are electrically coupled to a first plurality of CAM cells, said row comprising an NMOS pull-down transistor having a gate terminal that is electrically connected to the first word line segment, a first current carrying that is electrically connected to the first match line segment and a second current carrying terminal that is electrically coupled to either a pseudo-ground line associated with said row or a ground reference line (Vss).

56. A content addressable memory (CAM) array, comprising:

a first plurality of rows CAM cells that are partitioned into xR and xS segments; and

a match line control circuit that is disposed between the xR and xS segments, said match line control circuit comprising:

a plurality of latches that are configured to receive a first plurality of match line signals developed in the xR segment during a xR search operation; and

boolean logic that is electrically coupled to outputs of the plurality of latches, said boolean logic configured to evaluate match conditions represented by the first plurality of match line signals and conserve power by selectively blocking discharge of at least one precharged pseudo-ground line segment in the xS segment during a xS search operation when the match conditions indicate that no matching entries are present in the first plurality of rows of CAM cells in the xR segment during the xR search operation.

57. The CAM array of Claim 56, wherein the first plurality of rows of CAM cells in the xR segment share a common pseudo-ground line segment.

58. A content addressable memory (CAM) device, comprising:

a CAM array having a first row of CAM cells therein that comprises:

a first match line segment that is electrically coupled to a first segment of CAM cells in the first row;

a second match line segment that is electrically coupled to a second segment of CAM cells in the first row;

a pseudo-ground line segment that is electrically connected to the first and second segments of CAM cells; and

a match line signal repeater that is configured to detect and propagate a miss signal transition from the first match line segment to the second match line segment in-sync with a high-to-low transition of said pseudo-ground line segment during a search operation.

59. A content addressable memory (CAM) device, comprising:

a CAM array having a first plurality of columns that define a xR segment and a second plurality of columns that define a xS segment therein; and

a interface circuit extending between the xR and xS segments of said CAM array, said interface circuit comprising:

a segment-to-segment match line control circuit having a first plurality of latches therein that are configured to store match line information derived from the xR segment of said CAM array during a xR search operation; and

a segment-to-segment word line control circuit having a second plurality of latches therein that are configured to store word line information derived from the xR segment of said CAM array during a xR write operation.

60. The CAM device of Claim 59, wherein the first plurality of latches are responsive to at least a first capture control signal.

61. The CAM device of Claim 59, wherein the first plurality of latches are responsive to at least one capture control signal; and wherein the second plurality of latches are responsive to at least another capture control signal.

62. The CAM device of Claim 59, wherein said segment-to-segment match line control circuit further comprises a plurality of NMOS pull-down transistors having gate terminals that are electrically coupled to outputs of the first plurality of latches and drain terminals that are electrically coupled to respective xS match line segments within the xS segment of said CAM array.

63. The CAM device of Claim 58, wherein said segment-to-segment match line control circuit is configured to pass the stored match line information to the xS segment of said CAM array as active or inactive match line pull-down signals.

64. An integrated circuit memory device, comprising:

a content addressable memory (CAM) array block having at least two rows of CAM cells therein that are each partitioned into at least:

a lower xM row segment of CAM cells having a xM match line segment and xM word line segment associated therewith; and

an upper xN row segment of CAM cells having a xN match line segment and a xN word line segment associated therewith;

a match line control circuit that is configured to conserve power during a pipelined multi-cycle search operation by withholding pulling any of the upper xN match line segments high-to-low to thereby indicate a miss condition unless at least one partial match has been detected between a xM segment of an applied search word and partial entries in the lower xM row segments of CAM cells in the plurality of rows of CAM cells; and

a word line control circuit that is configured to pass at least one active word line signal from a lower xM word line segment associated with a first row of CAM cells to an upper xN word line segment associated with the first row of CAM cells during a pipelined multi-cycle write operation that is interleaved between two consecutive multi-cycle search operations.